WHAT IS CLAIMED IS:

1. A device for measuring signal skew, comprising:

a functional path extending from a circuit to an output terminal;

a logic gate placed within the functional path for receiving an output signal from the circuit on one input of the logic gate and an expected output signal on another input of the logic gate; and

a latch placed within the functional path for receiving an output of the logic gate and forwarding the output of the logic gate from the latch onto the output terminal during times when the latch enters a transparent mode.

2. The device as recited in claim 1, wherein the circuit comprises an integrated circuit and the output terminal comprises a bonding pad.

3. The device as recited in claim 1, further comprising a second logic gate coupled to receive the expected output signal and a test characterization enable signal, wherein the second logic gate forwards the expected output signal to the logic gate whenever the test characterization enable signal is active.

4. The device as recited in claim 3, wherein the logic gate is coupled to forward a match signal to the latch during times when the test characterization enable signal is active, and the output signal and the expected output are at the same logic value, and wherein the logic gate is coupled to forward the output signal to the latch during times when the test characterization enable signal is inactive.

5. The device as recited in claim 4, wherein the latch is coupled to forward the match signal or the output signal onto the output terminal during times when the latch enters the transparent mode by activating a gate terminal of the latch with a plurality of clock signal edges delayed in time with respect to each other.

6. The device as recited in claim 1, wherein the expected output signal transitions to an active state at a predetermined time when essentially no skew occurs on the output signal as measured on the output terminal.

7. The device as recited in claim 6, wherein the latch is coupled to forward the match signal onto the output terminal when the output signal transitions to the active state, preceded in time by the expected output signal transitioning to the active state.

8. A device for measuring access time and signal skew at an output terminal of a circuit, comprising:

a first series-connected logic gate and latch coupled to receive a clock signal forwarded to the circuit, and to latch a transition of a clock signal;

a second series-connected logic gate and latch coupled to receive an output signal from the circuit and an expected output signal, and to latch a transition of the output signal; and

a delay measurement device coupled to the output terminal for measuring the time difference between the transition of the clock signal and the transition of the output signal.

9. The device as recited in claim 8, wherein the latch of the first series-connected logic gate and latch comprises a pair of inputs, one of which is coupled to receive the clock signal and the other is coupled to receive a power supply voltage.

10. The device as recited in claim 8, wherein the latch of the second series-connected logic gate and latch comprises a pair of inputs, one of which is coupled to receive the output signal and the other is coupled to receive the expected output signal during times when the expected output signal is enabled.

11. The device as recited in claim 8, further comprising another logic gate coupled to receive the expected output signal and a test characterization enable signal, and to forward the expected output signal to the second series-connected logic gate and latch whenever the test characterization enable signal is active.

12. The device as recited in claim 8, wherein the delay measurement device is configured to produce the expected output signal at a predetermined time and to produce a plurality of clock signal edges successively delayed in time from an initial time to an ending time.

13. The device as recited in claim 12, wherein the latches of the first and second series-connected logic gates and latches receive the plurality of clock signal edges on a gated input of the latches for placing the transition of the output signal onto the output terminal at a measured time coinciding with one of the clock signal edges that occur between the initial time and the ending time.

14. The device as recited in claim 8, wherein the delay measurement device is configured to measure the access time as the time difference between the transition of the clock signal and the transition of the output signal.

15. The device as recited in claim 8, wherein the delay measurement device is configured to measure the signal skew as the time difference between a transition of the clock signal and the transition of the output signal.

16. A method for measuring signal skew, comprising:

latching a transition of a clocking signal;

forwarding the clocking signal to a circuit;

using the clock signal to produce an output signal from the circuit;

latching a transition of the output signal; and

measuring the signal skew as a time difference between a transition of the clocking signal appearing on an output terminal and when the transition of the output signal occurs on the output terminal.

17. The method as recited in claim 16, wherein said latching a transition of the clocking signal comprises recording when the transition of the clocking signal occurred.

18. The method as recited in claim 16, wherein said latching a transition of the output signal comprises recording when the transition of the output signal occurred relative to when the transition of the clocking signal occurred.

19. The method as recited in claim 16, further comprising activating a test characterization enable signal to enable the steps of latching the transition of the output signal and measuring the signal skew.

20. The method as recited in claim 16, further comprising deactivating a test characterization enable signal to disable the steps of latching the transition of the output signal and measuring the signal skew.